A MESFET Variable-Capacitance Model for GaAs Integrated Circuit Simulation

TOHRU TAKADA, KIYOYUKI YOKOYAMA, MASAO IDA, AND TSUNETA SUDO

Abstract—A simple MESFET capacitance model which has a clearly explained physical meaning for a wide bias voltage range has been developed for use in simulations of GaAs integrated circuits.

In this model, gate–source and gate–drain capacitances are represented by analytical expressions which are classified into three different regions for bias voltages: a before-pinch-off region including the neighborhood of the built-in voltage, an after-pinch-off region, and a transition region.

2-dimensional analysis results support the validity of the analytically derived capacitance model. The model is applicable to MESFET's used in integrated circuits that have low donor-thickness product.

I. Introduction

IN THE PAST few years, GaAs integrated circuits (IC's) fabricated from Schottky gate field effect transistors (MESFET's) have emerged as a promising technology for the development of high-speed digital circuits. For the design of IC's, a simple and accurate circuit simulation model is required.

Simplified analytical models for GaAs MESFET's have been reported [1], [2], [3]. However, a capacitance model suitable for normally off-type GaAs MESFET's, by which direct coupled FET logics (DCFL's) are constructed, has not been reported. In the DCFL's, the gate–source voltage V_{gs} of a MESFET varies widely from the neighborhood of the built-in voltage to the voltage which pinches off the channel. Therefore, the model should be valid in the wide bias voltage range for accurate logic simulation. In previous papers, the bias-voltage-dependent capacitance for the neighborhood of the built-in voltage and for the neighborhood of the pinch-off voltage have not been clarified.

This paper discusses the bias voltage dependent capacitances for GaAs MESFET's with a view toward deriving a simplified and reasonable capacitance model which is applicable to a wide bias voltage range. 2-dimensional analysis is also carried out in order to confirm the validity of the derived model.

The equivalent circuit of a GaAs MESFET is shown in Fig. 1. In this paper, we consider only C_{gs} and C_{gd} that are voltage dependent capacitances. The other capacitances determined by the parallel conductor spacing C_{gss}, C_{gds}, and C_{dss} have been calculated by Pucel *et al.* as capacitances independent of the internal space charge [3].

The devices studied here are GaAs MESFET's having low donor-thickness products of active layers ($\lesssim 1\times 10^{12}$ cm^{-2}), such as normally off MESFET's or normally on MESFET's with slightly negative threshold voltages. Since, in these MESFET's, the amount of stationary charge accumulation which exists under the drain-side edge of the gate is too small, it can be assumed that there is no effect of accumulation on the capacitance characteristics [4].

In the following sections, we consider the capacitances by classifying them into three regions: a before-pinch-off region with a built-in voltage nearby, an after-pinch-off region, and a transition region.

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II. Internal Gate–Source Capacitance C_{gs}

A. Before-Pinch-Off Region

Our calculation is based on the simplified charge distribution shown in Fig. 2 in order to discuss the low donor-thickness product FET. The internal space charge region can be divided into three sections, sections I, II, and III whose charge amounts are Q_1, Q_2, and Q_3, respectively. Internal gate–source capacitance C_{gs} is expressed as

$$C_{gs}=C_{gs1}+C_{gs2}+C_{gs3}=\left(\frac{\partial Q_t}{\partial V_s}\right)_{V_g-V_d=\text{const}} \tag{1}$$

where Q_t is the total space charge and

$$C_{gs1}=\left(\frac{\partial Q_1}{\partial V_s}\right)_{V_g-V_d=\text{const}} \tag{2}$$

$$C_{gs2}=\left(\frac{\partial Q_2}{\partial V_s}\right)_{V_g-V_d=\text{const}} \tag{3}$$

$$C_{gs3}=\left(\frac{\partial Q_3}{\partial V_s}\right)_{V_g-V_d=\text{const}} \tag{4}$$

Here, we assume that the depletion layer edge beneath the gate varies linearly from the source-side edge to the drain-side edge as shown in Fig. 2. In addition, we assume that the carrier concentration changes abruptly at the boundary of the depletion layer. Q_1 then becomes

$$Q_1=\frac{1}{2}qN_dWl_ga\left\{\left(\frac{V_{bi}-V_g+V_s}{V_p}\right)^{1/2}+\left(\frac{V_{bi}-V_g+V_d}{V_p}\right)^{1/2}\right\} \tag{5}$$

$$V_p=qN_da^2/(2\epsilon) \tag{6}$$

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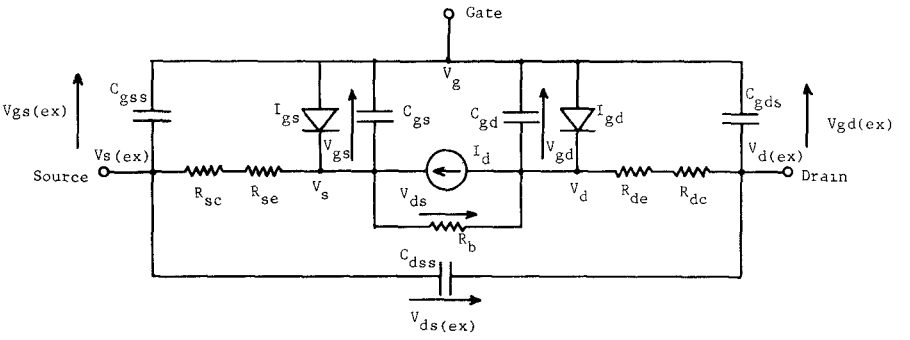

Fig. 1. MESFET equivalent circuit. R_{sc}: source ohmic resistance, R_{se}: gate-to-source resistance, R_{dc}: drain ohmic resistance, R_{de}: gate-to-drain resistance, R_b: leak resistance, I_d: channel current, I_{gs}: gate-to-source current, I_{gd}: gate-to-drain current, C_{gs}: internal gate–source capacitance, C_{gd}: internal gate–drain capacitance, C_{gss}: gate–source stray capacitance, C_{gds}: gate–drain stray capacitance, and C_{dss}: drain–source stray capacitance.

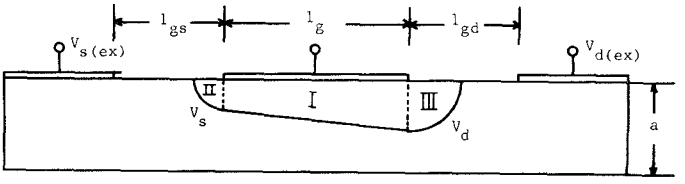

Fig. 2. Internal space charge distribution in the before-pinch-off region. l_g: gate length, l_{gs}: gate-to-source distance, l_{gd}: gate-to-drain distance, a: active layer thickness, V_g: gate potential, $V_{s(ex)}$: external source potential, $V_{d(ex)}$: external drain potential, V_s: internal source potential, and V_d: internal drain potential.

where q, N_d, W, V_{bi}, ϵ, and V_p are electron charge, carrier concentration of the active layer, gate width, built-in voltage, GaAs permittivity, and pinch-off voltage, respectively. From (2) and (5), we obtain

$$C_{gs1}=\frac{1}{2\sqrt{2}}\left(\frac{qN_d\epsilon}{V_{bi}-V_g+V_s}\right)^{1/2}\cdot Wl_g. \tag{7}$$

We also approximate that the charge distribution forms in sections II and III are quarter arcs. Q_2 and Q_3 are then given by

$$Q_2=\frac{\pi}{4}a^2qN_dW\frac{V_{bi}-V_g+V_s}{V_p} \tag{8}$$

$$Q_3=\frac{\pi}{4}a^2qN_dW\frac{V_{bi}-V_g+V_d}{V_p}. \tag{9}$$

Equations (3), (4), (8), and (9) are applied so that C_{gs2} and C_{gs3} become

$$C_{gs2}=\frac{\pi}{2}\epsilon W \tag{10}$$

$$C_{gs3}=0. \tag{11}$$

As a result, we obtain C_{gs} in the before-pinch-off region as

$$C_{gs}=\frac{\pi}{2}\epsilon W+\frac{Wl_g}{2\sqrt{2}}\left(\frac{qN_d\epsilon}{V_{bi}-V_g+V_s}\right)^{1/2}. \tag{12}$$

Equation (12) is an increasing function with the internal gate–source voltage V_{gs}; it shows a very large value when V_{gs} is in the neighborhood of V_{bi}.

We are interested in knowing whether (12) is reasonable or not whenever V_{gs} is high enough (near V_{bi}) for a gate-to-source current to flow significantly large. In order to clarify this point, we carried out 2-dimensional numerical analysis. The solid line in Fig. 3 is the 2-dimensional analysis result for an external gate–source capacitance $C_{gs(ex)}$ at 0 V $V_{ds(ex)}$ which is defined as

$$C_{gs(ex)}=\left(\frac{\Delta Q_t}{\Delta V_{s(ex)}}\right)_{V_{d(ex)}-V_g=\text{const}}. \tag{13}$$

In 2-dimensional analysis, we obtain the $C_{gs(ex)}$ instead of the C_{gs}. The device parameters used in the analysis are as follows:

$$l_g=l_{gs}=l_{gd}=1.0\ \mu\text{m},\ a=0.09\ \mu\text{m},$$

$$W=10\ \mu\text{m},\ N_d=1.0\times10^{17}\ \text{cm}^{-3},$$

$$\epsilon_s=12.6,\ R_{sc}=R_{dc}=0\ \Omega,\ V_{bi}=0.7\ \text{V}.$$

The result shows that the $C_{gs(ex)}$ obtained by 2-dimensional analysis in the before-pinch-off region increases with $V_{gs(ex)}$, then decreases above about 0.5 V. This bias voltage dependence is significantly different from that for C_{gs} in the neighborhood of V_{bi}. C_{gs} increases with V_{gs} even if V_{gs} is above 0.5 V.

The reason why the $C_{gs(ex)}$ decreases as $V_{gs(ex)}$ increased in a higher $V_{gs(ex)}$ region can be explained as follows: $C_{gs(ex)}$ is expressed from (1) and (13) as

$$C_{gs(ex)}\simeq C_{gs}\left(1-R_{se}\frac{\partial I_s}{\partial V_{gs(ex)}}\right) \tag{14}$$

where I_s is a source current (see Appendix I). Since I_s is equal to the gate current when $V_{ds(ex)}$ is 0 V, I_s is given as

$$I_s=I_0\{e^{q/kT(V_{gs(ex)}-R_{se}I_s)}-1\} \tag{15}$$

where I_0 is half the gate Schottky diode saturation current and q/kT is the thermal voltage. Thus, $\partial I_s/\partial V_{gs(ex)}$ in (14) becomes

$$\frac{\partial I_s}{\partial V_{gs(ex)}}=\left\{I_0\frac{q}{kT}e^{q(V_{gs(ex)}-R_{se}I_s)/(kT)}\right\}$$

$$/\left\{1+\frac{q}{kT}R_{se}I_0e^{q(V_{gs(ex)}-R_{se}I_s)/(kT)}\right\}. \tag{16}$$

Since (16) is a function approaching $1/R_{se}$ asymptotically,

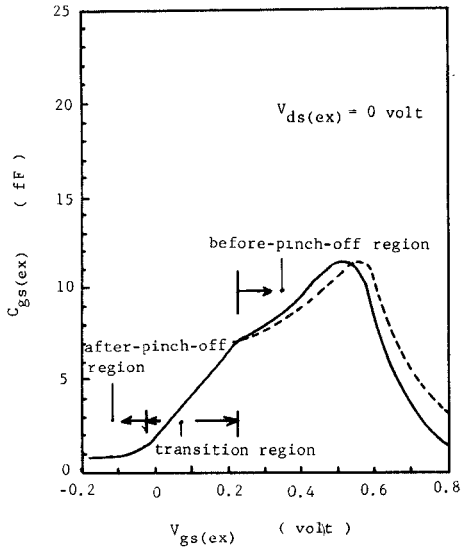

Fig. 3. External gate–source capacitance $C_{gs(ex)}$. ——is the $C_{gs(ex)}$ obtained by the 2-dimensional analysis and – – – – – is the $C_{gs(ex)}$ calculated by the C_{gs} model, $R_{se} = 200\ \Omega$.

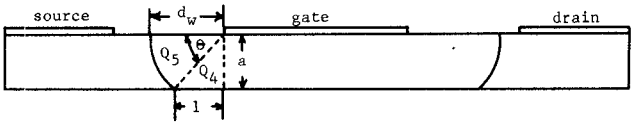

Fig. 4. Internal space charge distribution in the after-pinch-off region.

the parenthesis term in (14) approaches zero as $V_{gs(ex)}$ is increased. Therefore, the $C_{gs(ex)}$ is given as

$$C_{gs(ex)} = C_{gs}, \quad \text{at small } V_{gs(ex)}$$
$$C_{gs(ex)} = 0, \quad \text{at large } V_{gs(ex)}.$$

The broken line in Fig. 3 is the result calculated from (12), (14), and (16) using an R_{se} of 200 Ω which is obtained from a and l_{gs}. The calculated result of $C_{gs(ex)}$ obtained using (12) agrees relatively well with the $C_{gs(ex)}$ by the 2-dimensional analysis. Consequently, we can say that (12) is reasonable as an internal gate–source capacitance expression in the before-pinch-off region even if V_{gs} is in the neighborhood of the V_{bi}.

We notice from (12) that C_{gs} does not depend on the V_{ds}. In our 2-dimensional analysis, results showed that $C_{gs(ex)}$ increases as $V_{ds(ex)}$ is increased. However, this $C_{gs(ex)}$ increase with $V_{ds(ex)}$ is relatively small. For example, $C_{gs(ex)}$ for V_{ds} of 1.0 V at V_{gs} of 0.5 V is about 9 percent larger than $C_{gs(ex)}$ for V_{ds} of 0 V [5]. It is considered that this increase is mainly caused by the rise of V_s potential due to the R_{se} and drain current. Therefore, we can say as a first-order approximation that the internal gate–source capacitance C_{gs} does not depend on the V_{ds} as long as the nonaccumulation assumption holds true.

B. After-Pinch-Off Region

When the V_{gs} is decreased beyond threshold voltage V_{th}, the internal space charge distributes as shown in Fig. 4. Here, V_{th} is defined as

$$V_{th} \equiv V_{bi} - V_p. \tag{17}$$

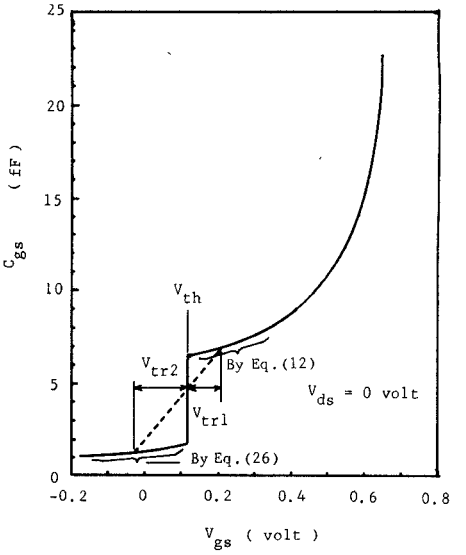

Fig. 5. The model of the internal gate–source capacitance.

In this voltage region, we can ignore the portion of C_{gs} directly under the gate because of the rapid advance of the depletion zone into the substrate. C_{gs} is then given by

$$\left.\begin{aligned} C_{gs} &= C_{gs4} + C_{gs5} \\ C_{gs4} &= \left(\frac{\partial Q_4}{\partial V_s}\right)_{V_g - V_d = \text{const}} \\ C_{gs5} &= \left(\frac{\partial Q_5}{\partial V_s}\right)_{V_g - V_d = \text{const}} \end{aligned}\right\} \tag{18}$$

where Q_4 and Q_5 are space charge amounts in the sections indicated in Fig. 4, which are expressed as follows:

$$Q_4 = qN_d W \frac{a}{2} l \tag{19}$$

$$l = \sqrt{d_w^2 - a^2} \tag{20}$$

$$d_w = \sqrt{\frac{2\epsilon}{qN_d}(V_{bi} - V_g + V_s)} \tag{21}$$

$$Q_5 = \pi d_w^2 \frac{\theta}{2\pi} qN_d W \tag{22}$$

$$\tan\theta = \frac{a}{l} = \sqrt{\frac{V_{bi} - V_{th}}{V_{th} - V_{gs}}}. \tag{23}$$

On the basis of (18), C_{gs4} and C_{gs5} are derived as

$$C_{gs4} = \frac{\epsilon w a}{2 \cdot l} \tag{24}$$

$$C_{gs5} = \frac{\epsilon w}{2}\left(2\theta - \frac{a}{l}\right). \tag{25}$$

Therefore, C_{gs} in the after-pinch-off region becomes

$$C_{gs} = \epsilon w \tan^{-1} \sqrt{\frac{V_{bi} - V_{th}}{V_{th} - V_{gs}}}. \tag{26}$$

The solid line in Fig. 5 shows the V_{gs} dependence of C_{gs} which is calculated using (12) and (26), using the same device parameters as in the 2-dimensional analysis.

Comparing the calculated C_{gs} from (26) in Fig. 5 (C_{gs} should be almost equal to $C_{gs(ex)}$ in principle because very small current flows) with the 2-dimensional analysis result in this region in Fig. 3, we note that the two results agree well in the lower V_{gs} region. However, the $C_{gs(ex)}$ obtained from the 2-dimensional analysis is larger than the C_{gs} from (26) above about -0.025 V V_{gs}. Therefore, (26) is applicable only in the following limited V_{gs} region:

$$\left.\begin{aligned} V_{gs} &< V_{th} - V_{tr2} \\ V_{tr2} &= 0.15 \text{ V} \end{aligned}\right\}. \tag{27}$$

C. Transition Region

In the study described above, (12) and (26) were reasonably derived physically for the before-pinch-off region and the after-pinch-off region, respectively. However, C_{gs} calculated from the two equations does not agree with $C_{gs(ex)}$ obtained by the 2-dimensional analysis in the vicinity of the V_{th} value of V_{gs} as shown in Figs. 3 and 5.

The disagreement is caused by an abrupt depletion layer assumption. Strictly speaking, the carrier concentration does not change abruptly at the boundary of the depletion layer due to the diffusion effect [6], [7]. Therefore, C_{gs} also does not change abruptly but changes gradually. Since the $C_{gs(ex)}$ change in the transition region in Fig. 3 is almost linear, we can model the C_{gs} in the transition region as the broken line drawn in Fig. 5. C_{gs} in this region then becomes

$$\begin{aligned} C_{gs} = {} & \epsilon w \tan^{-1}\sqrt{\frac{V_{bi}-V_{th}}{V_{tr2}}} \\ & + \left(\frac{\pi}{2}\epsilon w + \frac{l_g w}{2\sqrt{2}}\sqrt{\frac{qN_d\epsilon}{V_{bi}-(V_{th}+V_{tr1})}} \right. \\ & \left. - \epsilon w \tan^{-1}\sqrt{\frac{V_{bi}-V_{th}}{V_{tr2}}} \right) \\ & \cdot \{V_{gs}-(V_{th}-V_{tr2})\}/(V_{tr1}+V_{tr2}) \end{aligned} \tag{28}$$

where V_{tr1} and V_{tr2} are about 0.08 and 0.15 V, respectively. Since V_{tr1} and V_{tr2} are values dependent of the active layer carrier concentration, an additional investigation should be carried out if a more accurate simulation model is required.

III. Internal Gate–Drain Capacitance C_{gd}

The internal gate–drain capacitance C_{gd} is an important parameter which reflects the logic speed significantly due to the Miller effect.

If a charge accumulation at a drain-side edge under the gate does not occur or the amount of such accumulation is negligibly small, C_{gd} should be represented by the same expressions as C_{gs} since the drain and source are symmetric with respect to the gate. The previous C_{gd} model reported by Pucel *et al.* [3] is not represented by the same expression as C_{gs}. Although this model can be applied for large V_{ds} to show small C_{gd}, it cannot be used for smaller V_{ds}.

The nonaccumulation assumption is realized for the MESFET's used in integrated circuits, such as normally off

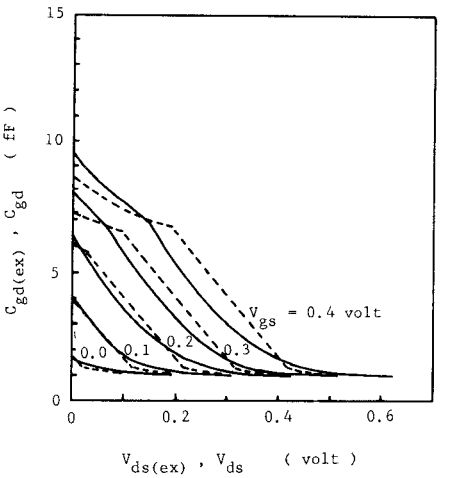

Fig. 6. ----- is the internal gate–drain capacitance C_{gd} versus internal drain–source voltage, V_{ds} (model). ——is the external gate–drain capacitance $C_{gd(ex)}$ versus external drain–source voltage $V_{ds(ex)}$ (2-dimensional analysis).

MESFET's or slightly normally on MESFET's. Thus, the C_{gd} expressions can be obtained, as follows, by replacing the V_{gs} by V_{gd} in (12), (26), and (28) described in Section II. For $V_{gd} > V_{th} + V_{tr1}$

$$C_{gd} = \frac{\pi}{2}\epsilon w + \frac{l_g w}{2\sqrt{2}}\left(\frac{qN_d\epsilon}{V_{bi}-V_{gd}}\right)^{1/2}. \tag{29}$$

For $V_{th} - V_{tr2} < V_{gd} < V_{th} + V_{tr1}$

$$\begin{aligned} C_{gd} = {} & \epsilon w \tan^{-1}\sqrt{\frac{V_{bi}-V_{th}}{V_{tr2}}} \\ & + \left(\frac{\pi}{2}\epsilon w + \frac{l_g w}{2\sqrt{2}}\sqrt{\frac{qN_d\epsilon}{V_{bi}-(V_{th}+V_{tr1})}} \right. \\ & \left. - \epsilon w \tan^{-1}\sqrt{\frac{V_{bi}-V_{th}}{V_{tr2}}} \right) \\ & \cdot \{V_{gd}-(V_{th}-V_{tr2})\}/(V_{tr1}+V_{tr2}). \end{aligned} \tag{30}$$

For $V_{gd} < V_{th} - V_{tr2}$

$$C_{gd} = \epsilon w \tan^{-1}\sqrt{\frac{V_{bi}-V_{th}}{V_{th}-V_{gd}}}. \tag{31}$$

When V_{gs} is constant, C_{gd} decreases as V_{ds} is increased, while C_{gs} does not change as V_{ds} is increased. C_{gd} as a function of V_{ds} calculated from (29), (30), and (31) is shown in Fig. 6 as broken lines. The external gate–drain capacitance $C_{gd(ex)}$ obtained by the 2-dimensional analysis, is shown in Fig. 6 as solid lines. Here, $C_{gd(ex)}$ is defined as

$$C_{gd(ex)} = \left(\frac{\Delta Q_t}{\Delta V_{d(ex)}}\right)_{V_g - V_{s(ex)} = \text{const}} \tag{32}$$

We found that the difference between C_{gd} and $C_{gd(ex)}$ increases with V_{gs}. It can be inferred that this difference is due to a voltage drop which results from a drain current I_d and gate-to-drain resistance R_{de}. Since the higher V_{gs} makes

the larger voltage drop due to the larger drain current, the difference between C_{gd} and $C_{gd(ex)}$ increases as V_{gs} is increased. Therefore, in principle, $C_{gd(ex)}$ should be almost equal to C_{gs} in the lower V_{gs} range because of the small drain current. C_{gd} obtained by our model in Fig. 6 shows good agreement with the 2-dimensional analysis results in the lower V_{gs} range. Consequently, it can be concluded that (29), (30), and (31) are reasonable enough to use as an accurate C_{gd} model.

IV. Conclusions

In order to obtain an accurate circuit simulation model of GaAs MESFET's used in integrated circuits, bias-voltage-dependent capacitances were investigated. The capacitance expressions were analytically derived by classifying them into three regions for bias voltages: before-pinch-off, after-pinch-off, and transition regions.

The 2-dimensional analysis study was also carried out and its results agreed well in all bias-voltage regions with those calculated by the obtained model.

This model is applicable to GaAs MESFET's that have low donor-thickness products such as normally off MESFET's and slightly normally on MESFET's.

The important information obtained in the investigation is enumerated below.

1) The external gate–source (or external gate–drain) capacitance decreases with increased gate–source (gate–drain) voltage in the vicinity of the built-in voltage due to the gate-to-source (gate-to-drain) current flowing.

2) The internal gate–source (internal gate–drain) capacitance in the before-pinch-off region including the neighborhood of the built-in voltage can be expressed as an increasing function with gate–source voltage (gate–drain) which is obtained on the assumption of an abrupt depletion layer.

3) The internal gate–source (gate–drain) capacitance in the after-pinch-off region, which is almost equal to the external one, can be expressed as a function independent of the gate length.

4) The internal gate–source (gate–drain) capacitance in the transition region, which is almost equal to the external one, increases almost linearly with the gate–source (gate–drain) voltage. This characteristic is owing to the gradual change in the carrier concentration at the boundary of the depletion layer.

Appendix I

An incremental external source potential $V_{s(ex)}$ is defined as

$$\Delta V_{s(ex)} \equiv V_{s(ex)1} - V_{s(ex)2}.$$

Then, $C_{gs(ex)}$ and C_{gs} are expressed by

$$C_{gs(ex)} = \frac{\Delta Q_t}{\Delta V_{s(ex)}} = \frac{\Delta Q_t}{V_{s(ex)1} - V_{s(ex)2}}$$

$$C_{gs} = \frac{\Delta Q_t}{V_{s(ex)1} + I_{s1}R_{se} - \{V_{s(ex)2} + I_{s2}R_{se}\}}$$

where I_{s1} and I_{s2} are gate-to-source current at $V_{s(ex)} = V_{s(ex)1}$ and $V_{s(ex)} = V_{s(ex)2}$, respectively. From the above equations, the following relation is derived:

$$\frac{C_{gs(ex)}}{C_{gs}} = 1 + R_{se}\frac{I_{s1} - I_{s2}}{V_{s(ex)1} - V_{s(ex)2}} = 1 + R_{se}\frac{\Delta I_s}{\Delta V_{s(ex)}}.$$

Here,

$$V_{gs(ex)} = V_g - V_{s(ex)}$$

then,

$$\frac{\Delta I_s}{\Delta V_{s(ex)}} = -\frac{\Delta I_s}{\Delta V_{gs(ex)}}$$

is obtained. Consequently, $C_{gs(ex)}$ can be approximated as

$$C_{gs(ex)} \simeq C_{gs}\left(1 - R_{se}\frac{\partial I_s}{\partial V_{gs(ex)}}\right).$$

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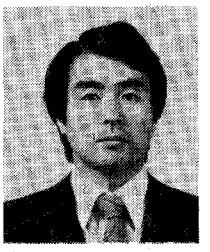

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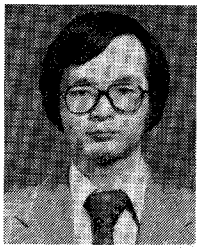

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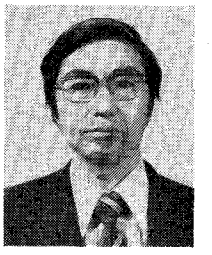

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Power Combiner with Gunn Diode Oscillators

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Abstract—**Combiners were developed using two Gunn diodes in dielectric waveguide (image line) oscillator circuits. The optimum configuration consisted of each Gunn diode being imbedded in a separate dielectric cavity as a primary source of oscillation. The dielectric resonators were then radiatively coupled to a common dielectric resonator from which the combined power could be obtained. It was found that the combined power was greater than the sum of the power obtainable from separate isolated oscillators. The proposed combiner appears attractive from the point of view of simplicity of construction and low cost and should be applicable to the millimeter-wave region, where the difficulties of precision machined metal-walled cavities are very great.**

I. INTRODUCTION

IN THE SEARCH for higher power semiconductor diode oscillator devices, the use of combiners has been suggested. Kurokawa [1] has published results with 12 packaged IMPATT diodes giving 10.5-W CW output at 9.1 GHz. He coupled individual coaxial oscillators to a main cavity from which the energy was extracted. He further found that it was important to have minimal coupling between the oscillators and also small coupling coefficient from the oscillator to the main cavity. The coaxial structures (housing the resonators) were separated by 1/2 wavelength and were individually tuned so that each resonator–diode combination would oscillate at the same frequency. Further work by Kurokawa [2] gave a detailed theory for the design of his combiner assembly.

Following these publications, due to the power limitations of IMPATT diodes, many investigations associated with millimeter waves have turned to investigating IMPATT diode combining techniques at 94 GHz and 140 GHz as the only means of obtaining adequate power [3] for radar applications using solid-state devices.

In this report, efforts were made to combine two Gunn diodes for approximately 10-GHz operation. Furthermore,

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